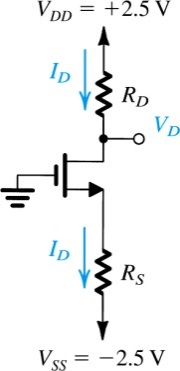
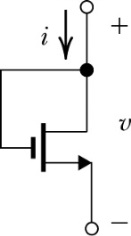
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**Example 5.3**

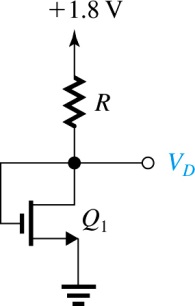
Design the circuit of Fig. 5.21, that is, determine the values of *RD* and *RS,* so that the transistor operates at *ID* = 0.4 mA and *VD* = +0.5 V. The NMOS transistor has *Vt* = 0.7 V, *nCox* = 100 A/V2*, L* = 1 m, and *W* = 32 m. Neglect the channel-length modulation effect (i.e., assume that ** = 0).

**Figure 5.21** Circuit for Example 5.3.

**Example 5.4**

Figure 5.22 shows an NMOS transistor with its drain and gate terminals connected together. Find the *i-v* relationship of the resulting two terminal device in terms of the MOSFET parameters *kn* = *k’n*(*W/L*) and *Vtn*. Neglect channel-length modulation (i.e.  = 0). Note that this two-terminal device is known as a **diode-connected transistor**.

**Figure 5.22**

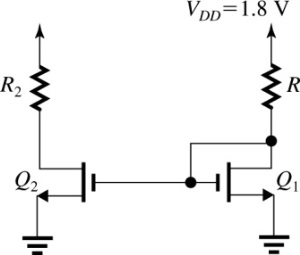


**Exercise 5.9**

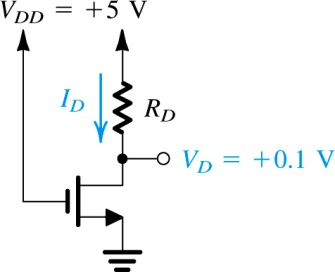
For the circuit in Fig. E5.9, find the value of *R* that results in *VD* = 0.8 V. The MOSFET has *Vtn* = 0.5 V, *nCox* = 0.4 mA/V2, *W/L* = 0.72 m/0.18 m, and ** = 0.

**Figure E5.9**

**Exercise 5.10**

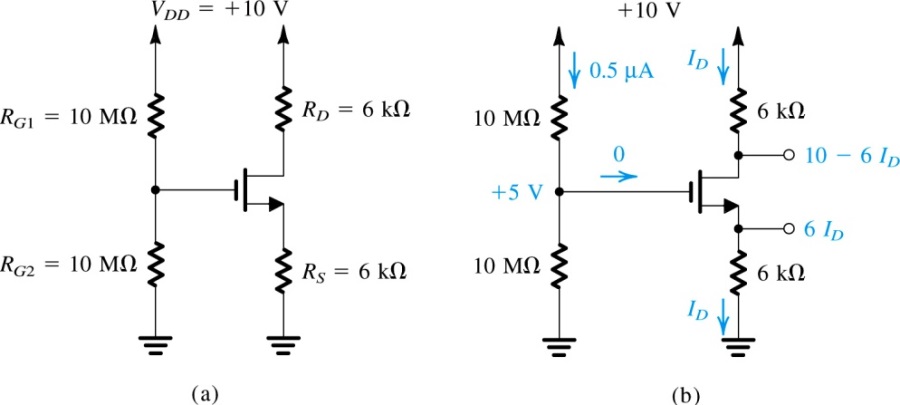
Figure E5.10, shows a circuit obtained by augmenting the circuit of Fig E5.9 considered in Exercise 5.9 with a transistor *Q*2 identical to *Q*1 and a resistor *R*2. Find the value of *R*2 that results in *Q*2 operating at the edge of the saturation region. Use your solution to Exercise 5.9.

**Figure E5.10**

**Example 5.5**

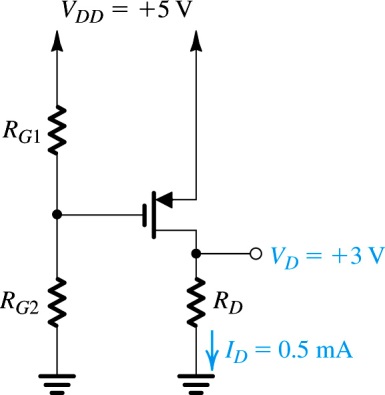
Design the circuit in Fig. 5.23 to establish a drain voltage of 0.1 V. What is the effective resistance between drain and source at this operating point? Let *Vtn*  = 1 V and *k’n*(*W/L*) = 1 mA/V2.

**Figure 5.23** Circuit for Example 5.5.

**Example 5.6**

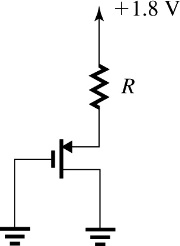
Analyze the circuit shown in Fig. 5.24(a) to determine the voltage at all nodes and the currents through all branches. Let *Vtn*  = 1 V and *k’n*(*W/L*) = 1 mA/V2. Neglect the channel-length modulation effect (i.e., assume that ** = 0).

**Figure 5.24 (a)** Circuit for Example 5.6.

**Example 5.7**

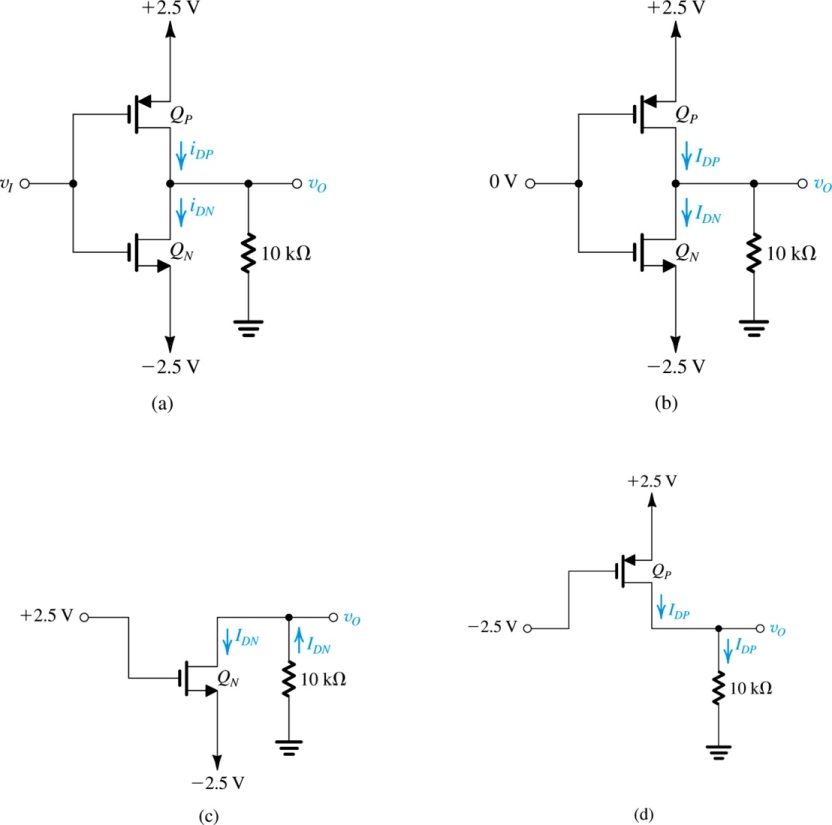
Design the circuit of Fig. 5.25 so that the transistor operates in saturation with *ID* = 0.5 mA and *VD* = +3 V. Let the enhancement-type PMOS transistor have *Vtp*  = -1 V and *k’p*(*W/L*) = 1 mA/V2. Assume ** = 0. What is the largest value that *RD* can have while maintaining saturation-region operation?

**Figure 5.25** Circuit for Example 5.7.

**Exercise 5.14**

For the circuit in Fig. E5.14, find the value of *R* that results in the PMOS transistor operating with an overdrive voltage |*VOV*| = 0.6 V. The threshold voltage is *Vtp* = -0.4 V, the process transconductance parameter *k’p* = 0.1 mA/V2, and the *W/L* = 10 m/0.18m.

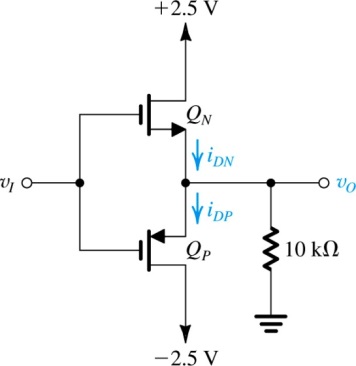
**Figure E5.14**

**Example 5.8**

The NMOS and PMOS transistors in the circuit of Fig. 5.26(a) are matched, with *k’n*(*Wn/Ln*) = *k’p*(*Wp/Lp*) = 1 mA/V2  and *Vtn* = -*Vtp* = 1 V. Assuming ** = 0 for both devices, find the drain currents *iDN* and *iDP*, as well as the voltage *vO*, for *vI* = 0 V, +2.5 V, and – 2.5 V.

**Figure 5.26** Circuits for Example 5.8.

**Exercise 5.15**

The NMOS and PMOS transistors in the circuit of Fig. E5.15 are matched, with *k’n*(*Wn/Ln*) = *k’p*(*Wp/Lp*) = 1 mA/V2  and *Vtn* = -*Vtp* = 1 V. Assuming ** = 0 for both devices, find the drain currents *iDN* and *iDP*, as well as the voltage *vO*, for *vI* = 0 V, +2.5 V, and – 2.5 V.

**Figure E5.15**